REMARKS

The Office Action dated October 13, 2005 has been received and its contents carefully considered.

This Amendment revises claims 1, 9, and 20 to claim the invention more specifically. It also revises claim 20 in response to a rejection for indefiniteness, and modifies several claims depending from claim 20 in order to conform them to the new wording of claim 20. Finally, this Amendment makes revisions in various claims to improve their form under U.S. claim-drafting practice. Claims 1, 9, and 20 are the independent claims. Claims 1-36 are now pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claim 20 has been rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. The Office Action asserts that this claim contains the word "pseudo" that is not enabled, not defined anywhere in the specification, and is first mentioned in claim 20. In response, claim 20 has been amended to replace the word "pseudo" with "dummy." This change in terminology is supported by paragraph [0031] of the application as-filed, which states that "when the neural network is in learning, the basis weights are obtained according to both the environmental parameters and the output vector that are set by the neural network itself, and when the neural network is in application, the output vector is determined according to the actual environmental parameters and the basis weights." Paragraph [0031] later sates that "the output vector and the environmental parameters during the learning procedure are a dummy output vector and dummy environmental parameters, which are used for learning the most suitable basis

weights." Accordingly, it is respectfully submitted that claim now 20 complies with the enablement requirement and the rejection of claim 20, as amended, should be withdrawn.

Claims 1-36 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Lin et al (U.S. patent. 6,163,583; hereinafter called simply "Lin") in view of Feng, Hewlett, and Alon.

Applicants' independent claim 1, as amended, recites:

> A method for changing a frequency of a central processing unit (CPU) under the control of a neural network of a computer system, comprising:
>
> providing a plurality of environmental parameters that affect usage rate of the CPU with respect to components of the computer system when the CPU operates at a first frequency based on an external frequency;
>
> calculating an output vector by inputting the environmental parameters to the neural network, wherein the output vector is determined according to a weighted sum of a plurality of basis vectors based on the environmental parameters;
>
> determining a clock multiplier factor according to the output vector; and
>
> changing the frequency of the CPU according to the output vector by enabling the CPU to operate at a second frequency according to the clock multiplier factor and the external frequency.

In contrast, Lin discloses a dynamic clocking apparatus 106 including a clock divider circuit 204, a multiplexer 206, and a finite state machine circuit 208. The clock divider circuit 204 receives a first clock 202 of frequency F1 and generates a second clock

210 of frequency F2 less than or equal to the frequency F1. (See column 3, line 61 through column 4, line 24).

Lin's multiplexer receives the first and second clocks 202 and 210 and ground 218 as inputs. These three inputs are selected in accordance with a two-bit select signal supplied over lines 216 from the finite state machine circuit 208. (See column 4, lines 38-47)

With continuing reference to the Lin reference, the finite state machine circuit 208 receives a bus request signal over line 212 indicating external access from the processor 102. An asserted bus request signal of line 212 indicates to the finite state machine circuit 208 a condition that requires the processor 102 to run at the slower second clock speed 210 when external memory access operations are to be performed. On the other hand, a deasserted bus request signal of line 212 requires the processor 102 to run at the higher first clock 202 speed, wherein the processor 102 deasserts the bus request signal of line 212 when the external access operation ends. (See column 4, line 48 through column 5, line 17)

The finite state machine circuit 208 of Lin's Figure 2 generates a select signal on lines 216 corresponding to the states 301, 302, and 303 of Figure 3. The run state 301 corresponds to the faster first clock 202 speed that is triggered by a deasserted bus request signal of line 212. The external state 303 corresponds to the slower second clock 210 speed and is actuated by the assertion of the bus request signal of 212. The hold state 302 is used for enabling the multiplexer 206 to select the ground input signal of line 218. (See column 5, line 32 to column 6, line 12)

In summary, the Lin reference discloses that a finite state machine circuit 208 controls the multiplexer 206 to select one of the three inputs; that is, the higher frequency F1, the slower frequency F2, or the ground signal, as the internal clock 220 to the CPU. In particular, **whether the bus request signal 212 is asserted or deasserted** determines how Lin's finite state machine circuit 208 generates the select signal on line 216 to control the multiplexer 206 **to output either frequency F1 or F2 or ground as the internal clock signal 220**. This contrasts with the invention defined by claim 1, in which **a plurality of environmental parameters that affect usage rate of the CPU with respect to components of the computer system** are provided when the CPU operates at a first frequency based on an external frequency, and **an output vector is calculated by inputting the environmental parameters to the neural network, wherein the output vector is determined according to a weighted sum of a plurality of basis vectors based on the environmental parameters.**

In particular, Lin does not disclose or suggest that an output vector is determined according to a weighted sum of a plurality of basis vectors based on environmental parameters and that a clock multiplier factor is determined according to the output vector, wherein the frequency of the CPU is changed according to the output vector by enabling the CPU to operate at a second frequency according to the clock multiplier factor and an external frequency.

In rejecting claim 1, the Office Action takes the position that Lin discloses "calculating an output vector by inputting the environment parameters to the neural network" (column 4, lines 44-47). To support this position, the Office Action provides an

Examiner's Note (EN) asserting that the finite state machine is the neural network, and that Alon teaches that every finite state machine can be built as a neural network (Abstract). However, the cited passage does not mention any features as recited in claim 1, as amended. The cited passage in Lin merely says:

> "These three inputs are selected in accordance with a two-bit select signal supplied over lines 216 provided from the finite state machine circuit 208."

This teaching does not disclose or otherwise suggest the features as recited in amended claim 1, that **an output vector is calculated by inputting environmental parameters to a neural network, wherein the output vector is determined according to a weighted sum of a plurality of basis vectors based on the environmental parameters.**

With regard to the Examiner's Note and the reasoning, Applicants respectfully disagree. Alon teaches that any (deterministic) automation can be realized or simulated by a neural net of the original type specified by McCullough and Pitts. A finite state machine can be simulated by a neural network with a number of neurons with modifications, conditions, and restrictions, as discussed in Alon (see pages 508-513, Figure 4). The finite state machine itself, as disclosed by Lin, is not a neural network. Although Lin teaches a finite state machine, Lin does not teach or suggest the use of a neural network in Lin's dynamic clocking apparatus. In addition, one may ask how Lin's finite state machine circuit 206 would be modified or replaced by a neural network circuit.

Furthermore, according to MEPE §2143.01, the prior art must suggest the desirability of the claimed invention, and obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

However, in rejecting claim 1, the Office Action provides no teaching, suggestion, or motivation to do so. On the other hand, Alon does provide the **disapproving conclusion** that "**parallel <u>hardware</u>** inspired by this somewhat primitive neural model **is unlikely to host arbitrary finite automata with uniform high efficiency**: Some automata will require networks that require about as many neurons as the automata have states!" (Emphasis added; see page 496 of the Alon paper, second paragraph.) In addition, Alon admits that "a **careful reading of this paper may produce the impression** that more complicated neural network models will suffer from **the same inherent inefficiency**." (Emphasis added; again, see the second paragraph on page 496.)

As discussed above, Lin discloses **a finite state machine circuit 208**, that is, a hardware circuit, to implement the states disclosed in Lin's Figure 3. With reference to Alon, one of ordinary skill in the art at the time of the invention would **disapprove of** the use of a neural network to replace **a finite state machine circuit** since Alon gives a negative impression with respect to efficiency in hardware implementation. Thus, the prior art does not suggest the desirability of the claimed invention.

For at least the above reasons, the method as recited in amended claim 1 is not rendered obvious over Lin in view of Alon. Moreover, since claims 2-9 depend from

claim 1, claims 2-9 also are not rendered obvious over Lin in view of Alon. Accordingly, the rejection of claims 2-9 should be withdrawn.

Regarding independent claims 9 and 20, the Office Action uses Lin as the primary reference and rejects claims 9 and 20 as being obvious over Lin in view of Feng. It is noted that claims 9 and 20 include features similar to those of claim 1. Claims 11-19 depend from claim 9, and claims 21-36 depend from claim 20. The cited secondary reference of Feng fails to disclose or even suggest the features recited in claim 9 and 20 (claim 1) that are missing from Lin. In addition, there is no suggestion or motivation provided to modify the teaching of Lin and use the neural network disclosed in Feng to arrive at the claimed invention, as claims 9 and 20 require. Therefore, claims 9-19 and 20-36 are patentable over the cited references for at least the reasons advanced above as to the patentability of independent claim 1, as well as having additional features recited therein. It is therefore respectfully submitted that the rejection should be withdrawn.

Conclusion

For the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,

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